Amendments to the Specification:

Please replace paragraph **[0042]** with the following amended paragraph:

[0042] Referring again to **Figure 4**, an embodiment of deserializer 405 includes a frequency and phase lock unit 430, a data rate detection unit 420, a frequency selector unit 435, and a frequency configuration unit 440. Data line 415 represents the incoming data stream received from a remote LAN or WAN network (not shown). Data line 415 take the form of conventional data transfer mediums, such as a data bus. Data rate detection unit 420 samples the phase rate of the incoming data stream and determines the rate of data transfer, e.g. 10.31 GHz or 9.95 GHz. The determined data rate is then conveyed to the frequency configuration unit ~~440~~ 425, which coordinates the process of locking to the incoming data stream by managing frequency selector unit 435 and frequency and phase lock unit 430. In one embodiment, dual external reference oscillators (clocks) 480 and 490 are provided to generate a plurality of reference frequencies that may be used to phase lock the incoming data stream. In one embodiment oscillator 480 generates WAN frequencies and oscillator 490 generates LAN frequencies.

Please replace paragraph **[0049]** with the following amended paragraph:

[0049] **Figure 5** is a schematic showing one embodiment of a SERDES device 500, which includes a serializer 504 and a deserializer 505. In **Figure 5**, the SERDES device is shown configured for a 10.31 GHz LAN network. In this configuration, the CMU ~~502~~ 510 is in the x66 or x132 mode. The PCS transmit rate can be clocked directly off the 156.25 MHz reference clock and the deserializer may generate output clocks at both the parallel data rate and a 3.125% slower (/4 or /8) PCS clock. Optionally, the CMU's can be configured in the x16, the x64 or the x128 mode (WAN configuration). In this configuration, the reference clock frequency should be increased by 3.125%. Box X02 is a WAN reference clock. Box X01 is a LAN reference clock. Tables 1 and 2, below provide various clock frequencies that may be associated with various embodiments of the present invention.